



SCS Engineering Release Notice

Phase14 Pre-Alpha Release Version 2.00.57.00 - SAS2XP86_Phase14.0 (SCGCQ00265894)

(SCGCQ00265894) - Phase14 Pre-Alpha Release Version 2.00.57.00 - SAS2XP86 Phase14.0



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Change Summary (Defects=1 Enhancements=3)

SCGCQ00265873 (CSET) - F/W Diagnostic Buffer post fails

SCGCQ00265872 (CSET) - Windows driver string addition for new custom OEM Mustang-based HBA

SCGCQ00265882 (CSET) - Update Custom OEM HBA driver string change for ALL Windows drivers

SCGCQ00265896 (CSET) - Correct hardware IDs for Intel Scotch Valley driver in Isinodrv.inf for ALL Windows drivers



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Total Defects Resolved (1)

(SCGCQ00265873 - Port of SCGCQ00228344)		Defect 1/1
HEADLINE:	F/W Diagnostic Buffer post fails	
DESC OF CHANGE:	<p>In LsiMpiPartitionMemory our NonCachedExtension is broken up into many memory blocks. Two of these blocks are BOOLEAN arrays (character arrays) sized to the number of MaxPersistentEntries (from IOCFacts). In the SAS Gen2 F/W, this value has been 0x80 (maintained 4-byte alignment), but in the SAS Gen3 F/W this value is 0x7F. When these two arrays were sized using that value, the alignment was off by 2 bytes. This caused the subsequent allocation of F/W diag buffers to not be on a 4-byte alignment.</p> <p>To fix this, when each of these arrays are sized, the allocated size is bumped up to the next 4-byte boundary to maintain a 4-byte alignment.</p>	
TO REPRODUCE:	<p>Using an Invader A0 eval board and the LSI_SAS3-2.50.51 driver, set the DriverParameter string for LSI_SAS3 to:</p> <p>EnaDiag=1;TBufSize=2097152;TImmed=1;</p>	
ISSUE DESC:	<p>Reboot the system and capture a F/W ring buffer via the UART. The debug of the F/W Diag Buffer Post message will show a physical address that is not 4-byte aligned, so the buffer post will fail.</p> <p>When the LSI_SAS3 driver is set (via registry entries) to post a F/W diagnostic buffer, the buffer post fails and no F/W diag information can be retrieved.</p> <p>F/W debug information shows that the physical buffer address specified in the Diag Buffer Post message is not aligned on a 4-byte boundary. The MPI 2.5 specification states that the F/W diag buffers being posted must be aligned on a 4-byte boundary.</p>	



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Total Enhancements Implemented (3)

(SCGCQ00265872 - Port of SCGCQ00248657)

Enhancement 1/3

HEADLINE: Windows driver string addition for new custom OEM Mustang-based HBA

NEW FUNCTIONALITY: Added the PnP ID and device description strings as necessary for the custom OEM Mustang-based HBA.

(SCGCQ00265882 - Port of SCGCQ00250995)

Enhancement 2/3

HEADLINE: Update Custom OEM HBA driver string change for ALL Windows drivers

NEW FUNCTIONALITY: In all of the LSI_SAS2.INF files, changed the custom OEM description string to the proper value.

(SCGCQ00265896 - Port of SCGCQ00250997)

Enhancement 3/3

HEADLINE: Correct hardware IDs for Intel Scotch Valley driver in Isinodrv.inf for ALL Windows drivers

NEW FUNCTIONALITY: Changed the PnP ID for the custom OEM enclosure to the proper hardware ID value.