

ReleaseOrder ID: DCSG02094613

Headline: GCA Release: CtrlFw_GIT_Ph_39.0 - 39.00.00.00 Firmware

Release Version: 39.00.00.00

UCM Project: CtrlFw_GIT

Sub UCM Project: CtrlFw_GIT_Ph_39.0

UCM Stream:

Release Type: GCA

State: Released

Release Baseline: Release-CtrlFw_GIT_Ph_39.0-39.00.00.00-2026.07.28.00.03.11

Release Date: 2026-07-28 07:02:46.000000

Date Generated: Aug 04, 2026

GCA Release Advisory

- Release Advisory From ReleaseOrder DCSG02094613 (GCA Release: CtrlFw_GIT_Ph_39.0 - 39.00.00.00 Firmware):

Release History

- [DCSG02093620 - ReleaseCandidate Release: CtrlFw_GIT_Ph_39.0 - 38.250.10.00 Firmware](#)
- [DCSG02086793 - ReleaseCandidate Release: CtrlFw_GIT_Ph_39.0 - 38.250.09.00 Firmware](#)
- [DCSG02082132 - Beta Release: CtrlFw_GIT_Ph_39.0 - 38.250.08.00 Firmware](#)
- [DCSG02074909 - Beta Release: CtrlFw_GIT_Ph_39.0 - 38.250.07.00 Firmware](#)
- [DCSG02067633 - Beta Release: CtrlFw_GIT_Ph_39.0 - 38.250.06.00 Firmware](#)
- [DCSG02061327 - Alpha Release: CtrlFw_GIT_Ph_39.0 - 38.250.05.00 Firmware](#)
- [DCSG02048178 - Alpha Release: CtrlFw_GIT_Ph_39.0 - 38.250.04.00 Firmware](#)
- [DCSG02044566 - Pre-Alpha-2 Release: CtrlFw_GIT_Ph_39.0 - 38.250.03.00 Firmware](#)
- [DCSG02037386 - Pre-Alpha-2 Release: CtrlFw_GIT_Ph_39.0 - 38.250.02.00 Firmware](#)
- [DCSG02024913 - Pre-Alpha-1 Release: CtrlFw_GIT_Ph_39.0 - 38.250.01.00 Firmware](#)

ReleaseOrder ID: DCSG02093620 [Open In CQWeb](#)

Headline: ReleaseCandidate Release: CtrlFw_GIT_Ph_39.0 - 38.250.10.00 Firmware

Release Version: 38.250.10.00

UCM Project: CtrlFw_GIT

Sub UCM Project: CtrlFw_GIT_Ph_39.0

UCM Stream:

Release Type: ReleaseCandidate

State: Released

Release Baseline: Release-CtrlFw_GIT_Ph_39.0-38.250.10.00-2026.07.24.01.41.11

Release Date: 2026-07-24 08:40:31.000000

Date Generated: Aug 04, 2026

Defects Fixed (1):

ID: DCSG02092645

Headline: MCTP commands with payload fail when wrong byte count field is set in I2C header

Description Of Change: Added a workaround to ignore the extra 3 bytes in the MCTP command payload.

Issue Description: In a recent fix a check was added to verify the payload length in MCTP header and byte count field in I2C header to avoid buffer overflow while copying the payload to local buffer for processing. OEM BMC was not setting the byte count field in I2C header properly and sending 3 extra bytes in the payload causing MCTP command with payload to fail.

Steps To Reproduce: Flash latest controller Firmware and observe failure in MCTP commands send by OEM BMC.

ReleaseOrder ID: DCSG02086793 [Open In CQWeb](#)

Headline: ReleaseCandidate Release: CtrlFw_GIT_Ph_39.0 - 38.250.09.00 Firmware

Release Version: 38.250.09.00

UCM Project: CtrlFw_GIT

Sub UCM Project: CtrlFw_GIT_Ph_39.0

UCM Stream:

Release Type: ReleaseCandidate

State: Released

Release Baseline: Release-CtrlFw_GIT_Ph_39.0-38.250.09.00-2026.07.06.02.39.18

Release Date: 2026-07-06 09:39:07.000000

Date Generated: Aug 04, 2026

Defects Fixed (2):

ID: DCSG02070864

Headline: PL fault E40E observed with Switch attached topology

Description Of Change: Marked the SES device on Switch as missing when the PCIe bar reconfiguration is performed so the IOs are blocked till discovery is run and the device is reinitialized.

Issue Description: During PCIe address reconfiguration the base address is cleared on all PCIe devices and task management is run on all PCIe devices. In case of Switch attached topology, the switch can also have one virtual SES device. IOs might start immediately after the PLI control request to start address reconfiguration is complete before the PCIe discovery could reconfigure the devices.

Steps To Reproduce: Perform PCIe address reconfiguration on a Switch attached topology.

ID: DCSG02084406

Headline: [SATA] Incorrect Request Sense response for drive in active power condition

Description Of Change: Clear the standby flag when start stop unit command is sent to SATA drive with start operation. Also only send the sense data to indicate drive is in standby when check power mode command completes with response set as standby.

Issue Description: Firmware sets a flag to indicate that the drive is in standby when a SCSI start stop unit command is sent to set the power condition as standby. This flag is not cleared when the start stop unit command is sent with start operation. This leads to incorrect sense response for request sense command.

Steps To Reproduce: Sent a start stop unit command to a SATA drive to change the power condition to standby. Send another start stop unit command with start operation. Send a request sense command and notice the response sense data indicates drive is in standby.

ReleaseOrder ID: DCSG02082132 [Open In CQWeb](#)

Headline: Beta Release: CtrlFw_GIT_Ph_39.0 - 38.250.08.00 Firmware

Release Version: 38.250.08.00

UCM Project: CtrlFw_GIT

Sub UCM Project: CtrlFw_GIT_Ph_39.0

UCM Stream:

Release Type:	Beta
State:	Released
Release Baseline:	Release-CtrlFw_GIT_Ph_39.0-38.250.08.00-2026.06.23.03.44.01
Release Date:	2026-06-23 10:43:47.000000
Date Generated:	Aug 04, 2026

Enhancements Implemented (1):

ID:	DCSG02080116
Headline:	Firmware downgrade gate
Description Of Change:	Added manufacturing page 20 to populate the minimum firmware version that can be downloaded. During Firmware download block and fail the firmware image download with version lower than the version in manufacturing page.

ReleaseOrder ID:	DCSG02074909 Open In CQWeb
Headline:	Beta Release: CtrlFw_GIT_Ph_39.0 - 38.250.07.00 Firmware
Release Version:	38.250.07.00
UCM Project:	CtrlFw_GIT
Sub UCM Project:	CtrlFw_GIT_Ph_39.0
UCM Stream:	
Release Type:	Beta
State:	Released
Release Baseline:	Release-CtrlFw_GIT_Ph_39.0-38.250.07.00-2026.06.03.23.37.49
Release Date:	2026-06-04 06:37:39.000000
Date Generated:	Aug 04, 2026

Defects Fixed (2):

ID:	DCSG02074104
Headline:	DDR Multibit ECC Errors
Description Of Change:	This compliments the changes in the DDR library made with DCSG02072000.
Issue Description:	ECC errors can occur in DDR with the right combination of Series 95xx controller chips from certain lots, voltage, temperature, and timing.
Steps To Reproduce:	Run IO and do temperature cycles.

ID:	DCSG02073590 (Port Of Defect DCSG02072000)
Headline:	DDR Multibit ECC Errors
Description Of Change:	A work around was implemented. Signals that are susceptible to glitching in the DDR phy are no longer used. This avoids the ECC errors.
Issue Description:	ECC errors can occur in DDR with the right combination of Series 95xx controller chips from certain lots, voltage, temperature, and timing.
Steps To Reproduce:	Run IO and do temperature cycles.

ReleaseOrder ID:	DCSG02067633 Open In CQWeb
Headline:	Beta Release: CtrlFw_GIT_Ph_39.0 - 38.250.06.00 Firmware
Release Version:	38.250.06.00
UCM Project:	CtrlFw_GIT
Sub UCM Project:	CtrlFw_GIT_Ph_39.0
UCM Stream:	
Release Type:	Beta
State:	Released
Release Baseline:	Release-CtrlFw_GIT_Ph_39.0-38.250.06.00-2026.05.12.03.04.12
Release Date:	2026-05-12 10:03:41.000000
Date Generated:	Aug 04, 2026

Defects Fixed (1):

ID:	DCSG02058405
Headline:	[SATA SMR] Report Zone data not swapped correctly in some cases
Description Of Change:	In case align data read is not possible reduced the chunk size and retry the read swap and write logic.
Issue Description:	While swapping the report zone data for SATA SMR drives the SGE's are cached in local buffer. The local buffer has 8 SGEs. In case the number of SGEs required are more than 8 the length is adjusted to be aligned with descriptor size. However if last SGE length is lesser than 64 it might not be possible to align the data.
Steps To Reproduce:	cannot reproduce the issue.

ReleaseOrder ID:	DCSG02061327 Open In CQWeb
Headline:	Alpha Release: CtrlFw_GIT_Ph_39.0 - 38.250.05.00 Firmware
Release Version:	38.250.05.00
UCM Project:	CtrlFw_GIT
Sub UCM Project:	CtrlFw_GIT_Ph_39.0
UCM Stream:	
Release Type:	Alpha
State:	Released
Release Baseline:	Release-CtrlFw_GIT_Ph_39.0-38.250.05.00-2026.04.29.00.19.49
Release Date:	2026-04-29 07:19:38.000000
Date Generated:	Aug 04, 2026

Defects Fixed (4):

ID:	DCSG02043525
Headline:	Invalid SEP DeviceHandle filled in Enclosure Page 0 for SEP SSP target device when an expander has SEP SSP target and SSP initiator devices
Description Of Change:	As per the new changes, the SEP Device Handle of the SEP SSP device is updated only when the expander's virtual PHYs are configured for SEP SSP devices.
Issue Description:	The SEP Device Handle field in Enclosure Page 0 for the SEP SSP target was overwritten with the device handle of the SSP initiator when the expander's first virtual PHY was configured as an SSP initiator and the following virtual PHY was configured as a SEP SSP target.
Steps To Reproduce:	1. Configure the expander's first virtual PHY as an SSP initiator and the following virtual PHY as a SEP SSP target. 2.Connect the expander to the 9500 controller. 3. Dump Enclosure Page 0 and observe that the SEP Device Handle for the SEP SSP device is incorrect.

ID:	DCSG02055696
Headline:	The controller firmware download reply status was not set to POR required when an SBR change was detected.
Description Of Change:	Updated the controller firmware download logic to set the reply status to Power On Reset required when an SBR change is detected during firmware download.
Issue Description:	During the code walkthrough, it was identified that the reply status was not being set to POR required upon detection of an SBR change.
Steps To Reproduce:	N.A

ID:	DCSG02050672 (Port Of Defect DCSG02049342)
Headline:	Fault 2674 seen while running libzbc suite on SMR drive
Description Of Change:	Clear the local SGE cache on completion of Report zone command Remove sge flag check which is causing out of bound access.

Issue Description: Since SGE cache is not cleared in case of report zone error scenario, PL is accessing stale data leading to the Fault.
Steps To Reproduce: run libzbc test suite

ID: DCSG02061284 (Port Of Defect DCSG02047121)
Headline: The drive aborts Read/Write I/Os with sense key 0Bh/4B04h.
Description Of Change: Reverted the combo SerDes firmware to the previous version.
Issue Description: After a WRITE command is sent to the drive, the controller receives an XFER_READY frame from the drive with a CRC error. As a result, the controller sends a NAK to the drive, followed by DATA frames. This sequence causes the drive to abort the WRITE command with sense key 0Bh/4B04h. This issue has been identified as a side effect of the latest combo SerDes firmware (0x6d80) and is not observed with the previous firmware version (0x6d00).
Steps To Reproduce: Run an I/O test on the 9650-16i controller with directly attached SAS drives.
Perform a reboot test on the controller.
Observe the I/O failure with sense key 0Bh/4B04h.

ReleaseOrder ID: *DCSG02048178* [Open In CQWeb](#)
Headline: *Alpha Release: CtrlFw_GIT_Ph_39.0 - 38.250.04.00 Firmware*
Release Version: *38.250.04.00*
UCM Project: *CtrlFw_GIT*
Sub UCM Project: *CtrlFw_GIT_Ph_39.0*
UCM Stream:
Release Type: *Alpha*
State: *Released*
Release Baseline: *Release-CtrlFw_GIT_Ph_39.0-38.250.04.00-2026.03.23.02.11.43*
Release Date: *2026-03-23 09:11:24.000000*
Date Generated: *Aug 04, 2026*

Defects Fixed (3):

ID: DCSG02035145
Headline: Data Abort exception was observed during concurrent I/O operations, drive hot-plug, and UBM firmware update operations.
Description Of Change: The issue has been resolved by initializing the global VSES device index only after the I2C bus reservation callback completes successfully and the bus reservation is confirmed.
Issue Description: The global VSES device index was initialized during the UBM firmware update and incorrectly set to an invalid value (0xFF) before invoking the I2C reservation callback. This resulted in memory corruption while accessing device context values.
Steps To Reproduce: 1. Connect two different UBM backplanes to the controller with all drives fully populated.
2. Start I/O operations on all 80 virtual drives.
3. Run I/O workloads on all virtual drives using I/O generation tools.
4. Simultaneously perform drive hot-plug operations on degraded arrays.
5. Concurrently initiate a UBM firmware upgrade or downgrade via BMC.

ID: DCSG02043376 (Port Of Defect DCSG02037307)
Headline: [SATA SMR] Report zone data is incorrect in some cases
Description Of Change: Changed the memory move function in report zone translation for SATA devices to read the exact amount of data requested and store the SGEs used in a separate cache which can be used to write the data after swapping the bytes.
Issue Description: For SCSI Report zone handling for SATA devices, the data received from drive in host memory needs to be read and byte swapped and written back to host. In case one of the SGE in the Scatter gather list has a length that is not aligned to size of descriptor in report zone data, there is a chance that the bye swap is not done for correct offset. This results in wrong data being sent for the report zone command.
Steps To Reproduce: Send a report zone command to SATA SMR drive in Windows OS, sometimes the data received is incorrect.

ID: DCSG02046658 (Port Of Defect DCSG01876528)
Headline: Controller fault 431E observed while running all phy off on test
Description Of Change: Made changes to ensure the hardware workaround is executed only for optical cable and does not run for internal controllers.
Issue Description: As per hardware team the work around earlier implemented to do second reset on the phys which did not linkup during phy off-on operation is specific to external controllers and does not apply for internal controllers. The workaround when run on internal controllers led to serdes fault.
Steps To Reproduce: 1) connected 9500-16i to SAS4X expander with Mixed SAS/SATA drives.
2) Start script which will do all phy off and on.
3) After few iterations observed controller fault 431E.

ReleaseOrder ID: *DCSG02044566* [Open In CQWeb](#)
Headline: *Pre-Alpha-2 Release: CtrlFw_GIT_Ph_39.0 - 38.250.03.00 Firmware*
Release Version: *38.250.03.00*
UCM Project: *CtrlFw_GIT*
Sub UCM Project: *CtrlFw_GIT_Ph_39.0*
UCM Stream:
Release Type: *Pre-Alpha-2*
State: *Released*
Release Baseline: *Release-CtrlFw_GIT_Ph_39.0-38.250.03.00-2026.03.10.02.49.51*
Release Date: *2026-03-10 09:49:12.000000*
Date Generated: *Aug 04, 2026*

Defects Fixed (2):

ID: DCSG02035986
Headline: Firmware incorrectly reports "SBR change detected(F). Diag Reset needed" when re-flashing the same firmware version.
Description Of Change: The SBR change message is now reported only when at least one section actually differs. When re-flashing the same firmware, that condition is false, so the message is no longer printed.
Issue Description: The code treated Diag Reset needed as true whenever the SBR match value had the RMC change only bits set, without requiring that any section actually differ. When all sections matched (same firmware, value 0x0F), that condition was still true, so the message was printed incorrectly.
Steps To Reproduce: 1. Flash Phase 37 firmware version 37.00.00.00
2. Reboot the system and verify that the running firmware version is 37.00.00.00.
3. Flash the same firmware image again.
4. During the flashing process, observe the message on the UART console.

ID: DCSG02036186
Headline: I2C Buffer overflow during the UBM controller firmware update (GET_NV_STORAGE_GEOMETRY) leads to PCIe quiesce state corruption and invalid memory access in the quiesce cancel path.
Description Of Change: Increased the I2C data buffer size to receive the Get Non-Volatile Storage Geometry command response data from the UBM device, as its size is larger than the currently allocated buffer.
Corrected the PCIe quiesce cancel logic to avoid using an uninitialized or NULL pointer when no managed switches are present on that root port.
Issue Description: During the UBM controller firmware update, the Get Non-Volatile Storage Geometry command requested more I2C receive data than the size of the shared receive buffer (128 bytes). This overflow corrupted adjacent memory, including the PCIe quiesce state, which led to invalid memory access in the PCIe quiesce cancel path when cancelling quiesce on a root port with no managed PCIe switches.
Steps To Reproduce: 1. Initiate the UBM controller firmware update via BMC and wait for completion.
2. Issue the Drive Power Disable command on an NVMe drive using the StorCli tool.
3. Observe the Data Abort exception on the controller UART console.

ReleaseOrder ID: *DCSG02037386* [Open In CQWeb](#)
Headline: *Pre-Alpha-2 Release: CtrlFw_GIT_Ph_39.0 - 38.250.02.00 Firmware*
Release Version: *38.250.02.00*
UCM Project: *CtrlFw_GIT*
Sub UCM Project: *CtrlFw_GIT_Ph_39.0*
UCM Stream:
Release Type: *Pre-Alpha-2*
State: *Released*
Release Baseline: *Release-CtrlFw_GIT_Ph_39.0-38.250.02.00-2026.02.23.01.09.58*
Release Date: *2026-02-23 09:09:48.000000*

Defects Fixed (1):

ID: DCSG02031646 (Port Of Defect DCSG01966307)
Headline: 9500-16i encountered firmware hang sometimes when BMC do system reset during IO testing to SATA HDD
Description Of Change: Added SAS core reset when SAS core fails to halt within timeout during chip reset.
Issue Description: While running IOs and performing chip reset, sometimes the SAS core is not able to halt during chip reset.
Steps To Reproduce: Attach few SATA drives to the controller and run IOs to the drives while parallely performing chip reset using BMC.

Enhancements Implemented (1):

ID: DCSG02022578
Headline: Change Duplicate MID Handling from Target Reset to Abort Task Set
Description Of Change: Update default NVDATA to set the Target Reset type for Duplicate Mid feature from Target Reset to Abort Task Set, to be compatible with multi path topologies.

ReleaseOrder ID: DCSG02024913 [Open In CQWeb](#)
Headline: Pre-Alpha-1 Release: CtrlFw_GIT_Ph_39.0 - 38.250.01.00 Firmware
Release Version: 38.250.01.00
UCM Project: CtrlFw_GIT
Sub UCM Project: CtrlFw_GIT_Ph_39.0
UCM Stream:
Release Type: Pre-Alpha-1
State: Released
Release Baseline: Release-CtrlFw_GIT_Ph_39.0-38.250.01.00-2026.01.21.00.07.19
Release Date: 2026-01-21 08:06:59.000000
Date Generated: Aug 04, 2026

Enhancements Implemented (1):

ID: DCSG02024856
Headline: Update the 95XX Firmware NVDATA version for Phase 39
Description Of Change: Updated the NVDATA major version to 39 for the Phase 39 95XX firmware.